in specific bit positions ("Fig. 6 LSB corresponds to specific bit position."). The Examiner is mistaken; FIG. 6 does not show placing information bits in a specific bit position. FIG. 6 is described in Yoshida at column 7, lines 17-32. As described in Yoshida, "FIG. 6 illustrates a situation when a block data is embedded in an image, one level (say "0") of a binarized data is expressed at a density which is the same as those of adjacent pixels, while the other level ("1" is expressed at a density which is different a little from those of adjacent pixels." Yoshida, column 7, lines 17-21. In Yoshida, information is not placed in any specific bit position, but rather, information is placed in a variety of different bit positions, which are influenced by adjacent pixels.

Since Yoshida does not describe placing information in specific bit positions of bit data as claimed by applicants, claims 1, 6 and 11 should be allowed. Claims 2-5, 7-10, and 12-15, which depend from claim 1, 6 and 11, also contain this limitation and should be allowed for at least the same reason. For the foregoing reasons, early action allowing the claims in this application is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 325772009100.

Respectfully submitted,

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